Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Withdrawn) A semiconductor device comprising:

a gate electrode formed extending on a first and second gate insulation films formed on first conductive type semiconductor substrate;

a second conductive type source region adjacent to one end of said gate electrode;

a first low concentration reverse conductive type drain region formed facing said source region through a channel region, having high impurity concentration peak at a position of the predetermined depth at least in said substrate under said first gate insulation film, and formed so that high impurity concentration becomes low at a region near surface of the substrate;

a second concentration reverse conductive type drain region formed so as to range to the first low concentration reverse conductive type drain region; and

a third concentration reverse conductive type drain region separated from the other end of said gate electrode and included in said second concentration reverse conductive type drain region.

2. (Withdrawn) A semiconductor device comprising:

a gate electrode formed extending on a first and second gate insulation films formed on first conductive type semiconductor substrate;

a second conductive type source region adjacent to one end of said gate electrode;

a first low concentration reverse conductive type drain region formed facing said source region through a channel region, having high impurity concentration peak at a position of the predetermined depth at least in said substrate under said first gate insulation film, and formed so that high impurity concentration becomes low at a region near surface of the substrate;

a second concentration reverse conductive type drain region formed so as to range to the first low concentration reverse conductive type drain region;

a third concentration reverse conductive type drain region separated from the other end of said gate electrode and included in said second concentration reverse conductive type drain region; and

a fourth concentration reverse conductive type layer formed so as to span from one end portion of said first gate insulation film to said third concentration reverse conductive type drain region.

3. (Withdrawn) A semiconductor device according to any of Claim 1 and Claim 2,

wherein said first insulation film is a field oxidation film field-oxidized.

4. (Withdrawn) A semiconductor device according to any of Claim 1 and Claim 2,

wherein said fourth concentration reverse conductive type layer has high impurity concentration peak at a position of the predetermined depth in said substrate at a region spanning from a position having the predetermined space from one end portion of said first gate insulation film to said third concentration reverse conductive type drain region, and is formed so that high impurity concentration becomes low at a region near surface of the substrate.

5. (Previously presented) A method of manufacturing a semiconductor device comprising:

implanting an impurity of a first conductive type in a semiconductor substrate of a second conductive type, wherein the implantation is a single implantation;

diffusing the implanted impurity in the substrate by providing a first gate insulation film on the semiconductor substrate by applying a heat treatment, so as to form a first drain region partially under the first gate insulation film and a second drain region adjacent to and above the first drain region, said first drain region having a different impurity concentration than the second drain region, wherein the first and second drain regions are formed by a single step of implanting the impurity and a single step of forming the first gate insulation by applying heat treatment;

providing a second gate insulation film on the semiconductor substrate except where the first gate insulation film is disposed;

providing a gate electrode that spans from the first gate insulation film to the second gate insulation film;

providing a source region of the first conductive type disposed proximally to one end of said gate electrode; and

providing a third drain region of the first conductive type disposed distally from the other end of said gate electrode and disposed in said second drain region.

6. (Previously Presented) A method for manufacturing a semiconductor device according to Claim 5, wherein said first drain region has a lower impurity concentration than the second drain.

7. (Previously presented) A method of manufacturing a semiconductor device according to Claim 5, further comprising:

providing a layer of the first conductive type to span a predetermined distance from one end of said first gate insulation film to and beyond said third drain region, wherein the layer is disposed over the second drain region.

8. (Currently Amended) A method of manufacturing a semiconductor device according to Claim 5, further comprising:

forming a layer of the first conductive type having a ~~high~~ middle impurity concentration at a predetermined depth in said substrate at a region spanning from a predetermined distance from one end of said first gate insulation film to and beyond said third drain region, wherein the layer is disposed over the second drain region.

9. (Previously presented) A method of manufacturing a semiconductor device according to Claim 7, wherein phosphorus ions are implanted with an energy of about 100 KeV to 200 KeV in the substrate to form the layer.

10. (Previously presented) A method of manufacturing a semiconductor device according to Claim 8, wherein phosphorus ions are implanted with an energy of about 100 KeV to 200 KeV in the substrate to form the layer.

11. (Previously presented) A method of manufacturing a semiconductor device according to Claim 7, wherein for forming the layer, ion implantation is carried out in a region spanning from a predetermined space from said first gate insulation film to said third drain region by using a photo-resist as a mask.

12. (Previously presented) A method of manufacturing a semiconductor device according to Claim 8, wherein for forming the layer, ion implantation is carried out in a region spanning from a predetermined space from said first gate insulation film to said third drain region by using a photo-resist as a mask.

13. (Previously presented) A method of manufacturing a semiconductor device according to Claim 7, wherein for forming the layer, ion implantation is carried out in a region spanning from a predetermined space from the first gate insulation film to said third drain region by using a side wall insulation film formed adjacent a side wall portion of said first gate insulating film as a mask.

14. (Previously presented) A method of manufacturing a semiconductor device according to Claim 8, wherein for forming the layer, ion implantation is carried out in a region spanning from a predetermined space from the first gate insulation film to said third drain region by using a side wall insulation film formed adjacent a side wall portion of said first gate insulating film as a mask.

15. (Previously presented) A method of manufacturing a semiconductor device according to Claim 7, wherein said layer is formed in a region spanning from a predetermined space from the first gate insulation film to said third drain region by using said first gate insulation film as a mask and ion-implanting obliquely from an upper side of the first gate insulation film.

16. (Previously presented) A method of manufacturing a semiconductor device according to Claim 8, wherein said layer is formed in a region spanning from a predetermined space from the first gate insulation film to said third drain region by using said first gate insulation film as a mask and ion-implanting obliquely from an upper side of the first gate insulation film.

17. (Previously presented) A method of manufacturing a semiconductor device according to Claim 7, wherein said layer is formed in a region spanning from a predetermined space from the first gate insulation film to said third drain region by using a photo-resist formed to cover said first gate insulation film and ion implanting obliquely from above the first gate insulation film.

18. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 8, wherein said layer is formed at a region spanning from a predetermined space from the first gate insulation film to said third drain region by forming a photo-resist formed to cover said first gate insulation film and ion implanting obliquely from above the first gate insulation film.

19. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 7, wherein said first drain region has a lower impurity concentration than said second drain region.

20. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 8, wherein said first drain region has a lower impurity concentration than said second drain region.

21. (Previously presented) A method of manufacturing a semiconductor device according to Claim 5, wherein the source region is in direct contact with the substrate.

22. (Previously presented) A method of manufacturing a semiconductor device according to Claim 7, wherein the layer of the first conductive type is formed after formation of the third drain region.

23. (Previously presented) A method of manufacturing a semiconductor device according to Claim 8, wherein the layer of the first conductive type is formed after formation of the third drain region.

24. (Previously presented) A method of manufacturing a semiconductor device according to Claim 7, wherein the layer of the first conductive type is formed through the second gate insulation film.

25. (Previously presented) A method of manufacturing a semiconductor device according to Claim 8, wherein the layer of the first conductive type is formed through the second gate insulation film.

26. (Previously presented) A method of manufacturing a semiconductor device according to Claim 7, wherein the layer of the first conductive type has a higher impurity concentration than the first or second drain regions and a lower impurity concentration than the third drain region.

27. (Previously presented) A method of manufacturing a semiconductor device according to Claim 8, wherein the layer of the first conductive type has a higher impurity

concentration than the first or second drain regions and a lower impurity concentration than the third drain region.